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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,370	03/14/2001	Daniel Charles Fiorella III	GIC-632	3341

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LAW OFFICE OF BARRY R LIPSITZ
755 MAIN STREET
MONROE, CT 06468

EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	4

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/808,370	FIORELLA ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/14/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2,3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on 03/14/2001.

Claims 1-14 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eckley (PCT: International Publication No. WO 92/12478) in view of Grundmann, "Flash Memory Technology and Techniques", Embedded System Conference 1999, Intel Corporation.

Given the broadest reasonable interpretation of followed claim in light of the specification:

As per claim 1:

Eckley discloses a transaction including a memory architecture (Re: Eckley: See page 5, line 18, 'memory device 101) that includes boot-up and accessible memory device 101-1 ('boot area') (Re: Eckley: See page 6, lines 12-15), one or more memory devices EEPROMs (Re: Eckley: See page 8, lines 18-20), and static RAM 101-3 (Re: Eckley: See page 6, lines 12-15).

In area of memory device 101-1 (claim limitation: 'boot area'), it includes code so called, 'vector table' (claim limitation: 'fixed vector table') (Re: Eckley: See page 7, lines 36-37, 'memory 101-1 may simply include a vector table') so that when executed to cause control (means: 'interrupting') transferring to vector table 101-3b (claim limitation: 'software vector table') in the static RAM (Re: Eckley: See page 7, lines 10-15), and code so called, 'initialization routine' (means: 'resetting') when executed to cause locating the commands and routines ('boot code') stored within memory device 101-1 (Re: Eckley: See page 8, lines 1-3).

In area of memory device 101-2 (claim limitation: 'non-volatile programmable read only memory'), it includes one or more EEPROMs (claim limitation: 'first application area and second application area') (Re: Eckley: See page 8, line 19) used for storing one or more modified versions (claim limitation: 'upgraded version of firmware') (Re: Eckley: See page 8, lines 30-31, 'modified versions of those commands and routines stored in memory devices 101-2').

In area of the static RAM (claim limitation: 'random access memory device'), it includes vector table 101-3b (claim limitation: 'software vector table') (Re: Eckley: See page 7, lines 10-15, 'one or more vector table 101-3b which is stored in the operating system data portion 101-3a of memory devices 101-3' (static RAM)).

The management of transaction executes the vector table in memory device 101-1 to cause control transferring to an address in vector table 103-3b. If an address value (old vector) in vector table 101-3 is modified to one of EEPROMs' locations (memory device 101-2) (means: 'filling the software vector table'), it redirects the memory access to the one of modified versions in memory device 101-2. Memory device 101-2 contains modified versions of memory 101-1 (means: 'loading the upgraded version') (Re: Eckley: See pages 9-10, started in page 9 at line 28 to page 10 in line 10, the description of how a modified version in the memory device 101-2 executed under address modification of vectors in the vector table 101-3b). Otherwise, it redirects to the commands and the initialization routines in memory device 101-1 (See FIGURE 1, referring to the redirecting pointer to 111 or 112).

Regarding limitation of claim 1:

Eckley discloses limitation "***providing a processor;***" (Re: Eckley: See page 10, lines 16-17, 'Motorola 68302 microprocessor'):

Eckley discloses limitation "***providing a non-volatile programmable read only memory device*** (Re: Eckley: See FIGURE 1, preferring to memory 101-1 and 101-2, where 101-2 is a programmable memory device) ***having a fixed vector table*** (Re: Eckley: See page 7, lines 36-37, 'memory 101-1 may simply include a vector table'), a ***boot area for storing boot code*** (Re: Eckley: See FIGURE 1, within the memory 101-1, and see page 7, line 38, 'the initialization routine'), ***a first application area for storing firmware*** (Re: Eckley: See page 8, lines 18-19, referring to 'more EEPROMs'), ***and a second application area for storing firmware"*** (Re: Eckley: See page 8, lines 18-19, referring to 'more EEPROMs')";

Eckley discloses limitation "***providing a random access memory device (RAM)*** (Re: Eckley: See FIGURE 1, memory 101-3) ***having a software vector table*** (Re: Eckley: See FIGURE 1, memory 101-3b, VECTOR TABLE(S)) and ***a RAM application area;***" (Re: Eckley: See FIGURE 1, memory 101-3 and memory 101-3a);

Eckley discloses limitation "***programming the fixed vector table*** (Re: Eckley: See page 7, lines 34-38, referring to 'a vector table' and 'initialization routine') ***with a reset vector address*** (Re: Eckley: See page 7, lines 34-38, 'initialization routine') ***and interrupt vector addresses*** (Re: Eckley: See page 7, lines 34-38, 'a vector table'), ***said reset vector address pointing to the boot code in said boot area*** (Re: Eckley: See pages 7-8, started with line 38 in page 7 to line 3 in page 8, 'initialization routine of memory device 101-1 may locate each command or subroutine ('boot code') stored within memory device 101-1) ***and said interrupt vector addresses pointing to corresponding interrupt vector addresses in the software vector table"*** (Re: Eckley: See page 7, lines 34-38, 'memory device 101-1 may simply include a vector table which is now is written into vector table 101-3b');

Eckley discloses limitation "***loading an upgraded version of firmware into one of the first application area or the second application area;***" (Re: Eckley: See page 8, lines 12-15, and 18-19, referring to 'stores modified versions of software' and 'one or more EEPROMs')

Eckley discloses limitation "***resetting the processor to run the upgraded version of firmware;***" (Re: Eckley: See FIGURE 1, redirecting pointer 112 to memory 101-2); and

Eckley discloses limitation "***filling the software vector tabl with proper corresponding interrupt vector address s for th interrupt vectors c ntained in the fixed vector table as determined by the upgraded version of firmware.***" (Re: Eckley: See FIGURE 1, address of vector table 101-3b-N, where the former address pointer 111, is redirected to the pointer to memory device 101-2; see page 10, lines 3-10).

Eckley, however, does not explicitly disclose a single device for such a limitation "*a non-volatile programmable read only memory device having a fixed vector table, a boot area for storing boot code, a first application area for storing firmware, and a second application area for storing firmware*". The difference is that Eckley does not combine memory device 101-1 and memory 101-2 into a single device as '*a non-volatile programmable read only memory device*' as of memory device 101-2.

Grundmann, discloses a single flash EEPROM or RPROM (Re: Grundmann: See page 4, left column, section Flash Cell Technology, referring to "EEPROM'; page 12, Figure 7, Single Flash) that replaces a ROM. The EEPROM can be partitioned (Re: Grundmann: page 12, Figure 7). It can store boot code and images (Re: Grundmann: page 13, left column, second bullet), and associate its code with the RAM for configuring data and performing interrupt handling/upgrading (Re: Grundmann: See page 12, right column, last paragraph, and see page 11, right column, first paragraph, 'the newest version written into block' and Figure 6).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to combine, the teaching "memory device 101-1 consisting a vector table for directing to a modified vector table, and initiation routines for locating commands within a ROM" and "one or more EEPROMs for storing upgraded versions" of Eckley, and the single flash EEPROM as disclosed by Grundmann.

The motivation is that the replacement for flash technology is unavoidable because of emerging flash EEPROM technology and its advantage of code-modifiable features. With the existing of a single flash EEPROM for replacing a ROM, it improves operating performance up-to-date without adding substantial cost of a computer product.

As per claim 2:

Regarding limitation, "***wherein the non-volatile programmable read only memory devic comprises a flash electrically erasable programmable read only memory device (FLASH)***":

Eckley discloses one or more non-volatile programmable read only memory (EEPROMs) (as mentioned in action of claim 1).

Eckley does not explicitly discuss the EEPROMS as being 'Flash'.

Grundmann, discloses a single flash EEPROM (Re: Grundmann: page 12, Figure 1).

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to further combine the teaching of Eckley "memory device 101-2: EEPROMs" and "memory 101-1" into the single flash EEPROM as disclosed by Grundmann.

The motivation is that taking advantage of emerging flash technology improves a product and manufactory flow.

As per claim 3:

Regarding limitation, "***wherein a prior version of firmware is running from one application area while the upgraded version of firmware is being loaded into the other application area***":

Eckley discloses the initialization is performed in memory device 101-1 and upgrading is performed into one or more EEPROMs (as cited in action of claim 1).

Eckley does not explicitly discuss a prior version of firmware is running from one application area while the upgraded version of firmware is being loaded into the other application area.

Grundmann, further discloses writing upgraded firmware by executing firmware from one part, while data is stored in another part of the single flash EEPROM (Re: Grundmann: page 10, right column, last paragraph).

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to further include the teaching "*running from one application area while the upgraded version of firmware is being loaded into the other application area*" as disclosed in Grundmann, into the EEPROMs' upgrading of Eckley.

The motivation is that it conforms to the requirement of firmware update for using running firmware code (code) to update code (data), where code and data in a single component (Flash memory).

As per claim 4:

Regarding limitation, "***A method in accordance with claim 1, further comprising: providing an erasable programmable memory device (EPROM) which is used to determine which application area will be accessed after the resetting step***".

Eckley discloses determining ***which application area will be accessed after the resetting step*** inherently in the use of 101-3b address values. For example, In the Eckley's passage, started from line 28 in page 9 to line 10 in page 10, it shows that one of EEPROMs (since memory device consists one or more EEPROMs) is accessed depending on a modified value in vector table 101-3b. Thus, after initialization, the execution knows which EEPROM to access.

Eckley does not disclose ***providing an erasable programmable memory device (EPROM)***; however, its suggestion is to include a PROM (or SRAM) in memory device 101-1 for purposes of power-up (Re: Eckley: see page 5, lines 31-32), where the execution of memory device 101-1 results to alter a vector table in the RAM for determining what part of memory device 101-2 is accessible.

Grundmann discloses an EPROM (Re: Grundmann: page 12, Figure 1).

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to further include an emergence of EPROM in flash technology as disclosed by Grundmann into the teaching of Eckley: memory area 101-1 that includes a PROM and deterring which part of memory 101-2 to be accessed.

The motivation is that it conforms to programmable properties of EPROM used for controlling and the availability of this chip which is provided for improving products.

As per claim 5:

Eckley discloses, "***A method in accordance with claim 1, further comprising: loading the RAM application area with data from the application area having the upgraded version of firmware***" (see page 3, lines 30-34, "(RAM) portion of the memory is used to store programs and data which are more likely to be altered').

As per claim 6: Eckley discloses, "***A method in accordance with claim 1, wherein: the first application area contains a first version of firmware; and the second application area contains a second version of firmware***" (Re: Eckley: see page 8, lines 18-19, 'one or more EEPROMs'. Thus, it discloses each EEPROM may store an upgraded version which is different from the version of another EEPROM).

As per claim 7: Regarding limitation, "***A method in accordance with claim 1, wherein said processor, said non-volatile programmable read only memory device, and said RAM are all provided in the form of a single integrated circuit***": Eckley discloses this limitation by providing a linear memory layout 101 (Re: Eckley: See FIGURE 1).

As per claim 8:

Claim 8 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 1. Therefore, Claim 8 is rejected in the same reason set forth in connecting to the rejection of Claim 1.

As per claim 9:

Claim 9 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 2. Therefore, Claim 9 is rejected in the same reason set forth in connecting to the rejection of Claim 2.

As per claim 10:

Claim 10 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 3. Therefore, Claim 10 is rejected in the same reason set forth in connecting to the rejection of Claim 3.

As per claim 11:

Claim 11 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 4. Therefore, Claim 11 is rejected in the same reason set forth in connecting to the rejection of Claim 4.

As per claim 12:

Claim 12 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 5. Therefore, Claim 12 is rejected in the same reason set forth in connecting to the rejection of Claim 5.

As per claim 13:

Claim 13 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 6. Therefore, Claim 13 is rejected in the same reason set forth in connecting to the rejection of Claim 6.

As per claim 14:

Claim 14 is an apparatus claim that has the functionality corresponding to the limitation recited in Claim 7. Therefore, Claim 14 is rejected in the same reason set forth in connecting to the rejection of Claim 7.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Spear et al., US No. 5,367,658, discloses an interrupt management method that allows the use ROM address space while still allowing access to software contained in the ROM.

Narayanaswamy et al., US No. 6,275,931 B1, discloses a memory system that allows different regions for holding boot code.

Rasmussen, US No. 6,640,334 B1, discloses a remotely updating firmware system that allows different regions for holding boot code.

Bell et al., GB 2 227 548 A, discloses a memeory system for holding patches.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be

reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers:

(703) 872-9306 (for formal communication intended for entry);

(703) 746-5429 (for informal or draft communication, please label "PROPOSED" or "DRAFT").

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TED T. VO

Patent Examiner
Art Unit: 2122

February 5, 2004